AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 4, line 17 with the following amended paragraph:

--In order to achieve the described objects, the present invention provides a method of filling a bit line contact via. First, a substrate having a device region and periphery region is provided. The device region has a transistor having a gate electrode, drain region, and source region, on the substrate. Then, a dielectric layer is formed overlying the substrate. The dielectric layer has a bit line contact via exposing the drain region, and periphery contact via exposing the periphery region. Next, a doped conductive layer, lower than the top surface of the gate electrode ~~dielectric layer~~, is formed overlying the drain region. Further, a barrier layer is conformally formed overlying the dielectric layer, doped conductive layer, and periphery region. Finally, a first conductive layer is formed filling the bit line contact via and periphery contact via.

Please replace the paragraph beginning on page 7, line 23 with the following amended paragraph:

--In Fig. 2G, a conductive layer 260 doped with an element in either group 13 (IIIA) or 15 (VA) of periodic table on all the exposed surface of substrate 200. The conductive layer 260 is preferably polycrystalline silicon doped with As. Dopants in conductive layer 260 can diffuse into drain region 212, resulting in decreasing the contact impedance of bit line contact when a doped conductive layer is ~~subsequently~~ conformally formed overlying the drain region 212, dielectric layer 230, and periphery region 203 ~~on drain region 212~~, and further maintaining the original ranges of drain region 212 and source region 214, thereby maintaining the designed electrical performance of device 201 and improving the electrical performance of the end product.

Please replace the paragraph beginning on page 8, line 5 with the following amended paragraph:

--In Fig. 2H, ~~the unwanted conductive layer 260 is removed by etching, remaining the conductive layer 260 lower than the bottom of via 231, contacting drain region 212.~~ the doped

conductive layer is etched to leave a remaining portion of the doped conductive layer 260 lower than the top surface of the gate electrode 220 overlying the drain region 212.